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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,092	12/05/2003	Chun-Chieh Lin	TSM03-0670	8814

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,092	LIN ET AL.	
	Examiner	Art Unit	
	Matthew E Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 22-55* is/are rejected.

7)☒ Claim(s) *19-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/24, 6/14, 10/12*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Election filed on October 11, 2004.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification does not disclose the limitations of claims 22 and 23.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 22 and 23 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not disclose how the gate dimensions relate to the carrier mobility in the channel region.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 6-10, 19, and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Currie et al. (US Pub. 2004/0026765 A1).

In re claim 1, Currie et al. shows (fig. 4) a semiconductor structure comprising: a semiconductor substrate that includes a first semiconductor material (411) and a second semiconductor material (412) wherein the first semiconductor material has a lattice constant that is different from a lattice constant of the second material [0014, lines 5-6]; a first transistor (300A) formed in the semiconductor substrate, the first transistor having first source and drain regions (340A) formed in the substrate oppositely adjacent a first channel region, wherein a first gate dielectric (320) overlies the first channel region and a first gate electrode (350A) overlies the first gate dielectric, and wherein the first channel region is formed in the first semiconductor material and at least a portion of the first source and drain regions are formed in the second semiconductor material; and a second transistor (300B) formed in the semiconductor substrate, having a conductivity type (N type) different than the first transistor, the second transistor having second source and drain regions (340B) in the substrate

oppositely adjacent a second channel region, wherein a second gate dielectric (320B) covers the second channel region and a second gate electrode (350B) covers the second gate dielectric.

In re claim 2, Currie discloses [0071] that first transistor is coupled to the second transistor to form an inverter.

In re claim 6, Currie discloses [0075] that the gate dielectric is formed from a high-k dielectric material.

In re claim 7, Currie shows (fig. 3) that the first and second gate electrodes comprise a metal material (352).

In re claim 8, Currie discloses [0014] the well known concept that SiGe has a higher lattice constant than Si. Therefore, the lattice constant of the second semiconductor material (412) is larger than the lattice constant of the first semiconductor material (411) because the second semiconductor material is made of SiGe and the first semiconductor material is made of Si.

In re claim 9, Currie discloses [0077] that the first transistor is a PMOS transistor.

In re claim 10, Currie discloses [0078] that the second semiconductor material comprises silicon (Si) and germanium (Ge).

In re claim 19, Currie shows (fig. 4) that a portion of the second source and drain regions are formed in a third semiconductor material (430).

In re claim 24, Currie discloses [0072 and 0078] that the source, drain, and gate electrodes of the first and second transistors each include a silicided portion.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-5, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Currie et al. (US Pub. 2004/0026765 A1) as applied to claim 1 above, and further in view of Fitzgerald et al. (US Pub. 2002/0125471 A1).

In re claims 3-5, Currie et al. shows all of the elements of the claims except the transistors begin coupled to form a NOR, NAND, or XOR circuit which Fitzgerald et al. discloses [0125]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the transistors of Currie by coupling them to form NOR, NAND, and XOR circuits as taught by Fitzgerald to provide optimized processing circuits with increased speed.

In re claims 22 and 23, as far as understood, Fitzgerald discloses [0073-0083, 0096] the relationship between the ratios of the gate width and the carrier mobility of the channel.

Claims 11-18 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Currie et al. (US Pub. 2004/0026765 A1) as applied to claims 1, 8, 9, and 10 above, and further in view of Yeo et al. (US Pub. 2004/0173815 A1).

In re claims 11 and 13, Currie et al. does not show that the second semiconductor material comprise, Si, Ge, and C. Yeo et al. discloses [0033] that a second semiconductor layer (mismatch zone 305b in fig. 3B) may comprises an alloy of silicon, germanium, and carbon. The silicon carbon alloy forms a zone having a lattice constant less than that of the silicon substrate (or first semiconductor material) and enhance the electron mobility in the channel region. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second semiconductor material of Currie by using a material comprising silicon, germanium, and carbon as taught by Yeo to enhance electron mobility in the channel of the transistor.

In re claim 12, the references do not specifically show that the concentration of germanium is greater than 10%. However, Yeo discloses [0031] that a silicon germanium alloy has "a natural lattice constant ...depending on the concentration of germanium in the silicon germanium alloy." It would have been obvious to one of ordinary skill in the art at the time the invention was made to add germanium in any silicon alloy having a desired concentration to form a material having a desired lattice constant. It has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

In re claim 14, Currie already shows (fig. 4) that one of the transistors is an NMOS transistor.

In re claim 15-18, Yeo discloses [0033] that the semiconductor material comprises silicon, germanium, and carbon. The concentration of carbon is in the range of 0.01 to 0.04 percent.

In re claim 35, none of the references show the specific distance between the junction and gate dielectric edge. Yeo discloses [0034] that lattice-mismatched zones (second semiconductor materials 305a and 305b) have a varying thickness which would ultimately affect the depth of the junction between the first and second semiconductor materials. It would have been obvious to one of ordinary skill in the art at the time the invention was made to space the first and second semiconductor junction and gate dielectric to a desired distance to arrange the active layer having a specific compressive or tensile stress. It has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 26-36 and 41-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akita et al. (US 6,256,239 B1) in view of Currie et al. (US Pub. 2004/0026765 A1).

In re claim 26, Akita et al. shows (fig. 11) an inverter comprising; a transistor (Tr_{19}) formed in the semiconductor substrate, the transistor having a source region and a drain region formed in a semiconductor substrate oppositely adjacent a channel region and a load element (13) formed in the semiconductor substrate, the load element coupled between the drain region and a first supply voltage node (Vdd). A second

supply voltage node (Vss) is coupled to the source region. Akita et al. shows all of the elements of the claims except the channel being formed in a first semiconductor material and at least a portion of the source region and the drain region is formed in a second semiconductor material, the first semiconductor material being different than the second semiconductor material. Currie et al. shows (fig. 3) a strained transistor having a channel region formed in a first semiconductor layer (311) and portions of source and drain (340) formed in a second semiconductor layer (312). With such a configuration improved channel performance is provided for both NMOS and PMOS transistors [0064, 0065, 0076]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the transistor channel of the inverter described by Akita by adding different semiconductor materials as taught by Currie to improve the channel performance of the device.

In re claims 27-29, Akita discloses that the load element comprises a resistor and the transistor comprises an NMOS or PMOS transistor (col. 6, lines 56-67 and col. 9, lines 11-20). The load element comprises a transistor as shown by the possible load elements in figs. 7(a-d).

In re claim 30, Currie discloses that a strained transistor may be used in an inverter [0071] and improve the channel performance of the device. When combined with Akita, the strained transistor of Currie would be substituted for the load transistor of Akita to improve the channel performance of that device

In re claims 31 and 32, Currie discloses that a high-k dielectric is used for the gate dielectric [0063] and that the gate electrode comprises metal [0072].

In re claims 33-35, Currie discloses [0014] the well known concept that SiGe has a higher lattice constant than Si. Therefore, the lattice constant of the second semiconductor material (412) is larger than the lattice constant of the first semiconductor material (411) because the second semiconductor material is made of SiGe and the first semiconductor material is made of Si. The first transistor is a PMOS transistor [0077].

In re claim 36, the references do not specifically show that the concentration of germanium is greater than 10%. However, Currie discloses [0065] that a "greater Ge concentration can also enhance hole mobility." It would have been obvious to one of ordinary skill in the art at the time the invention was made to add germanium in any silicon alloy having a desired concentration to enhance hole mobility. It has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

In re claim 41, Currie discloses [0072 and 0078] that the source, drain, and gate electrodes of the first and second transistors each include a silicided portion.

In re claims 42 and 43, Currie shows (fig. 3) that the first semiconductor material (311) consists essentially of silicon (tensile Si) and the second semiconductor (312) material comprises silicon and germanium (SiGe).

In re claim 45, Currie discloses [0016] that the substrate comprises an insulating layer underlying the first semiconductor material to form a SOI device.

In re claim 46, Currie discloses [0072 and 0078] that a conductive material of TaSi is formed over the source and drain regions

In re claims 47-55, Currie shows (fig. 3) that a gate dielectric (320) is formed over the channel and a gate electrode (351) of semiconductor material such as polycrystalline silicon is formed over the gate dielectric. Alternatively the gate electrode may be formed of a metal, silicide, and nitride [0072]. The gate dielectric may also comprise silicon oxide or a high dielectric material such as hafnium oxide [0063].

Claims 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akita et al. (US 6,256,239 B1) in view of Currie et al. (US Pub. 2004/0026765 A1) as applied to claim 26 above, and further in view of Yeo et al. (US Pub. 2004/0173815 A1).

In re claims 37-40, Currie et al. does not show that the second semiconductor material has a lattice constant smaller than the lattice constant of the first semiconductor material and may comprise, Si, Ge, and C. Yeo et al. discloses [0033] that a second semiconductor layer (mismatch zone 305b in fig. 3B) may comprises an alloy of silicon, germanium, and carbon. The silicon carbon alloy forms a zone having a lattice constant less than that of the silicon substrate (or first semiconductor material) and enhance the electron mobility in the channel region. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second semiconductor material of Currie by using a material comprising silicon, germanium, and carbon as taught by Yeo to enhance electron mobility in the channel of the transistor.

In re claims 38, Currie already shows (fig. 4) that one of the transistors is an NMOS transistor.

In re claim 40, Yeo discloses [0033] that the semiconductor material comprises silicon, germanium, and carbon. The concentration of carbon is in the range of 0.01 to 0.04 percent.

Allowable Subject Matter

Claims 19-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wang et al. (US 5,155,571) and Oda et al. also show transistor devices having mismatched semiconductor layers to enhance the channel performance of the device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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January 7, 2005

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